PLLs and their application in wireless communication systems

PLL synthesisers are part of almost any modern wireless communication device. While most of their components are usually integrated in an IC, the designer can strongly influence the performance by the design of the loop filter and the VCO.

This course enables engineers to understand the principles of PLL circuits and to design and characterise PLL synthesizers optimized for a given application.

Particular attention is paid to practical issues, such as:

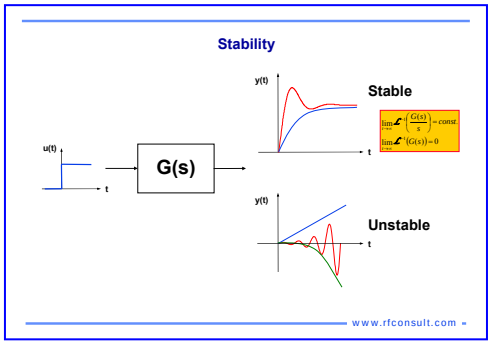
- Loop filter design based on lock time and spurious requirements
- Modulation concepts and their characteristics
- The impact of phase noise on the system performance
- Measurement of PLL parameters

The Course Schedule:

Day One

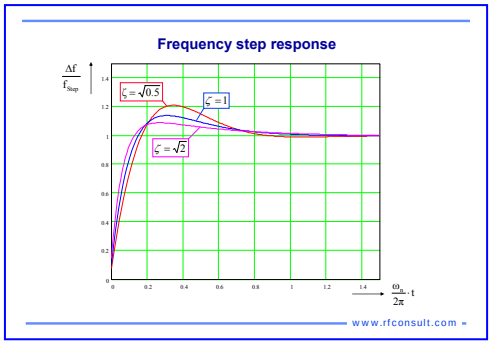
Control Loop Basics

- Open and closed loop gain and transfer functions
- Bode plot, phase margin, amplitude margin
- Poles and zeros, characteristic function
- Closed loop transfer function, bandwidth, dynamical control behaviour



PLL Components

- VCOs
- Phase noise in VCOs
- Phase detector types
- Charge pumps, speed-up
- Dividers and Mixers in a PLL



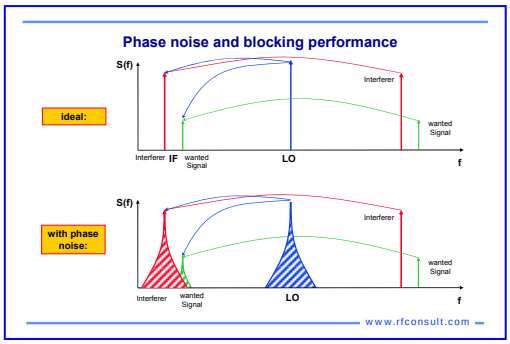
PLL Basics

- The phase transfer function
- Transfer functions for noise and spurious signals
- Lock time, ω_n, ξ and phase margin
- Typical loop filters
- Correlation between phase comparison frequency and loop bandwidth requirement
- Phase and frequency modulation of a PLL

Day Two

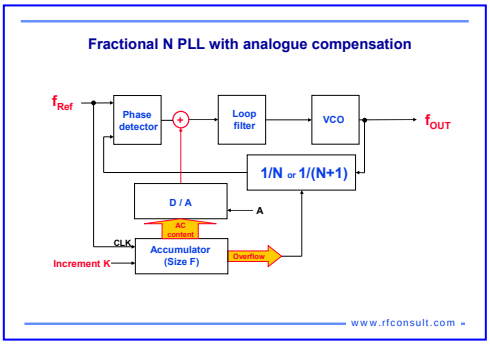
The PLL in a wireless system

- Correlation between phase and frequency error and SSB phase noise
- Effect of the phase noise on blocking and adjacent channel power performance
- Sources of phase noise in a PLL and its simulation



The Integer-N-PLL in a wireless system

- Loop filter calculation from lock time requirements
- Trade-off between spurs, noise and lock time
- Sources of PFD spurs
- The use of charge pumps, charge pump issues
- Problems linked to speed-up circuits



The Fractional-N-PLL in a wireless system

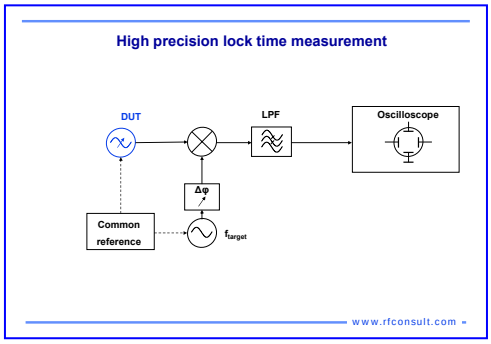
- Basics of operation
- Spurs due to the fractional concept
- Analogue and digital fractional compensation
- Limits of fractional compensation circuits
- The impact of phase detector linearity

The direct digital synthesiser DDS

- Concept, advantages and limitations
- System example: Combination with an integer-N-PLL

Measurement of PLL parameters

- Phase noise measurement with a spectrum analyser
- Phase noise measurement by down conversion
- Delayed self homodyne phase noise measurement
- Simple lock time measurement
- High precision lock time measurement
- Measuring the PLL phase transfer function



The participants will be provided with an extensive set of lecture notes.

For more information please contact:

RF Consult GmbH

Am Gasteig 3
D-83737 Irschenberg
E-Mail: contact@rfconsult.com
Tel: +49 8025 99 5000